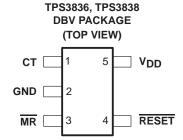
SGLS141A - DECEMBER 2002 - REVISED JANUARY 2007

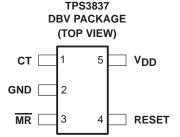
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Supply Current of 220 nA (Typ)
- Precision Supply Voltage Supervision Range: 1.8 V, 2.5 V, 3.0 V, 3.3 V
- Power-On Reset Generator With Selectable Delay Time of 10 ms or 200 ms
- Push/Pull RESET Output (TPS3836), RESET Output (TPS3837), or Open-Drain RESET Output (TPS3838)
- Manual Reset
- 5-Pin SOT-23 Package
- Temperature Range: -40°C to 125°C

description

The TPS3836, TPS3837, TPS3838 families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

- Applications Include
 - Applications Using Automotive Low-Power DSPs, Microcontrollers, or Microprocessors
 - Battery-Powered Equipment
 - Intelligent Instruments
 - Wireless Communication Systems
 - Automotive Systems





During power on, \overline{RESET} is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps \overline{RESET} output active as long as V_{DD} remains below the threshold voltage V_{IT} . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold voltage V_{IT} .

When CT is connected to GND a fixed delay time of typical 10 ms is asserted. When connected to V_{DD} the delay time is typically 200 ms.

When the supply voltage drops below the threshold voltage V_{IT}, the output becomes active (low) again.

All the devices of this family have a fixed-sense threshold voltage V_{IT} set by an internal voltage divider.

The TPS3836 has an active-low push-pull RESET output. The TPS3837 has active-high push-pull RESET, and TPS3838 integrates an active-low open-drain RESET output.

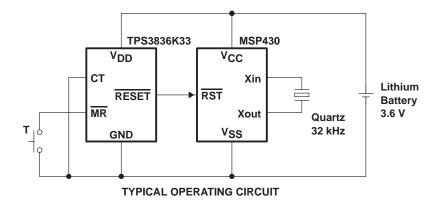


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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description (continued)



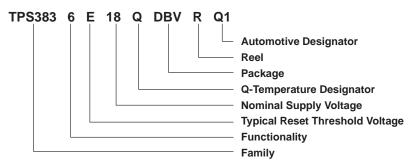
The product spectrum is designed for supply voltages of 1.8 V, 2.5 V, 3 V, and 3.3 V. The circuits are available in a 5-pin SOT-23 package. The TPS3836-Q-Q1, TPS3837-Q-Q1, TPS3838-Q-Q1 families are characterized for operation over a temperature range of –40°C to 125°C.

PACKAGE INFORMATION

TA	DEVICE NAME	THRESHOLD VOLTAGE	SYMBOL
	TPS3836E18QDBVRQ1 [†]	1.71 V	PDNQ
	TPS3836J25QDBVRQ1 [†]	2.25 V	PDSQ
	TPS3836H30QDBVRQ1 [†]	2.79 V	PHRQ
	TPS3836L30QDBVRQ1 [†]	2.64 V	PCAQ
	TPS3836K33QDBVRQ1 [†]	2.93 V	PDTQ
	TPS3837E18QDBVRQ1 [†]	1.71 V	PDOQ
-40°C to 125°C	TPS3837J25QDBVRQ1 [†]	2.25 V	PDRQ
	TPS3837L30QDBVRQ1 [†]	2.64 V	PCBQ
	TPS3837K33QDBVRQ1 [†]	2.93 V	PDUQ
	TPS3838E18QDBVRQ1 [†]	1.71 V	PDQQ
	TPS3838J25QDBVRQ1 [†]	2.25 V	PDPQ
	TPS3838L30QDBVRQ1 [†]	2.64 V	PCCQ
	TPS3838K33QDBVRQ1 [†]	2.93 V	PDVQ

[†]DBVR indicates tape and reel of 3000 parts.

ORDERING INFORMATION





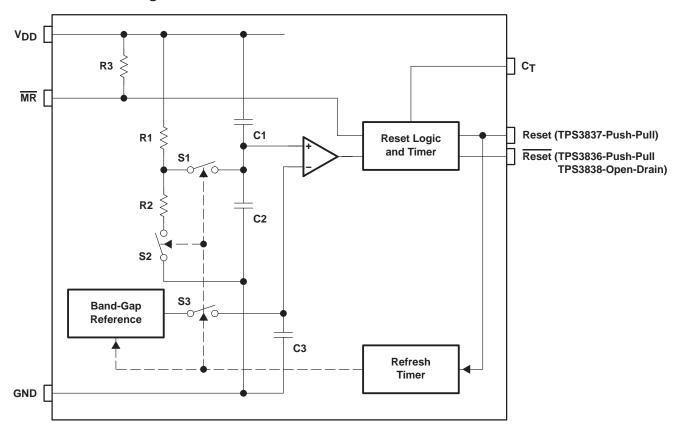
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FUNCTION TABLE TPS3836, TPS3837, TPS3838

MR	V _{DD} > V _{IT}	RESET [†]	RESET [‡]
L	0	L	Н
L	1	L	Н
Н	0	L	Н
Н	1	Н	L

†TPS3836 and TPS3838

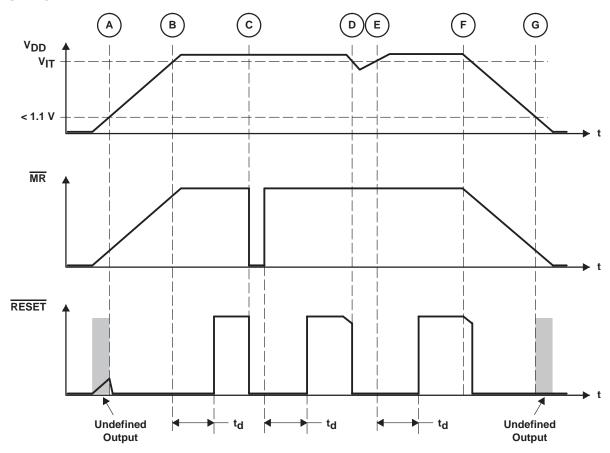
functional block diagram



[‡]TPS3837

TPS3836E18-Q1 / J25-Q1 / H30-Q1 / L30-Q1 / K33-Q1 TPS3837E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1, TPS3838E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1 NANOPOWER SUPERVISORY CIRCUITS SGLS141A - DECEMBER 2002 - REVISED JANUARY 2007

timing diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{DD} (see Note 1)	7 V
All other pins (see Note 1)	
Maximum low output current, I _{OL}	5 mA
Maximum high output current, IOH	
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A	–40°C to 125°C
Storage temperature range, T _{stq}	–65°C to 150°C
Soldering temperature	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than t=1000 h continuously

DISSIPATION RATING TABLE

PACKAGE	T _A <25°C	DERATING FACTOR	T _A = 70°C	T _A = 85°C	T _A = 125°C
	POWER RATING	ABOVE T _A = 25°C	POWER RATING	POWER RATING	POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW	87 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V _{DD}	1.6	6	V
Input voltage, V _I	0	V _{DD} + 0.3	V
High-level input voltage, V _{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage, V _{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at \overline{MR} , $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T _A	-40	125	°C



TPS3836E18-Q1 / J25-Q1 / H30-Q1 / L30-Q1 / K33-Q1 TPS3837E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1, TPS3838E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1 NANOPOWER SUPERVISORY CIRCUITS SGLS141A - DECEMBER 2002 - REVISED JANUARY 2007

electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CO	MIN	TYP	MAX	UNIT		
		RESET	$V_{DD} = 3.3 \text{ V},$	$I_{OH} = -2 \text{ mA}$				
.,	Libertarial autorituralitaria	(TPS3836)	$V_{DD} = 6 V$	$I_{OH} = -3 \text{ mA}$	0.8×			V
VOH	High-level output voltage	RESET	$V_{DD} = 1.8 V,$	$I_{OH} = -1 \text{ mA}$	V_{DD}			V
		(TPS3837)	$V_{DD} = 3.3 \text{ V},$	$I_{OL} = -2 \text{ mA}$				
		RESET	$V_{DD} = 1.8 V,$	$I_{OL} = 1 \text{ mA}$				
1/	Law lavel autout valtage	(TPS3836/8)	$V_{DD} = 3.3 V,$	$I_{OL} = 2 \text{ mA}$			0.4	V
VOL	Low-level output voltage	RESET	$V_{DD} = 3.3 V$,	$I_{OL} = 2 \text{ mA}$			0.4	V
		(TPS3837)	$V_{DD} = 6 V$,	$I_{OL} = 3 \text{ mA}$				
	Davis vin vasat valta na	TPS3836/8	$V_{DD} \ge 1.1 V$,	$I_{OL} = 50 \mu A$			0.2	
	Power-up reset voltage (see Note 2)	TPS3837	V _{DD} ≥ 1.1 V,	I _{OH} = -50 μA	0.8 × V _{DD}			V
		TPS383xE18			1.64	1.71	1.76	
		TPS383xJ25			2.16	2.25	2.30	
VIT	Negative-going input threshold voltage (see Note 3)	TPS383xH30			2.70	2.79	2.85	V
	voltage (see Note 3)	TPS383xL30			2.54	2.64	2.71	
		TPS383xK33			2.82	2.93	3.10	
			1.7 V < V _{IT} < 2.5 V			30		
V _{hys}	Hysteresis at V _{DD} input		2.5 V < V _{IT} < 3.5 V			40		mV
			3.5 V < V _{IT} < 5 V			50		
lн	High-level input current	MR (see Note 4)	$\overline{\text{MR}} = 0.7 \times \text{V}_{\text{DD}},$	V _{DD} = 6 V	-40	-60	-100	μΑ
		СТ	$CT = V_{DD} = 6 V$		-25		25	nA
IIL	Low-level input current	MR (see Note 4)	MR = 0 V,	V _{DD} = 6 V	-130	-200	-340	μΑ
	·	СТ	CT = 0 V,	V _{DD} = 6 V	-25		25	nA
loH	High-level output current	TPS3838	$V_{DD} = V_{IT} + 0.2 V,$	$V_{OH} = V_{DD}$			25	nA
I _{DD} Supply current			V _{DD} > V _{IT} ,	V _{DD} < 3 V		220	500	~ ^
			$V_{DD} > V_{IT}$	V _{DD} > 3 V		250	550	nA
		V _{DD} < V _{IT}			10	25	μΑ	
	Internal pullup resistor at MR					30		kΩ
Cl	Input capacitance at MR, CT		$V_I = 0 V \text{ to } V_{DD}$			5		pF

NOTES: 2. The lowest voltage at which $\overline{\text{RESET}}$ output becomes active. $t_{\Gamma_{\tau}} V_{DD} \ge 15 \,\mu\text{s/V}$

4. If manual reset is unused, MR should be connected to V_{DD} to minimize current consumption.

^{3.} To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.

TPS3836E18-Q1 / J25-Q1 / H30-Q1 / L30-Q1 / K33-Q1 TPS3837E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1, TPS3838E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1 NANOPOWER SUPERVISORY CIRCUITS SGLS141A - DECEMBER 2002 - REVISED JANUARY 2007

timing requirements at R_L = 1 M Ω , C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS			TYP	MAX	UNIT
		at V _{DD}	$V_{IH} = V_{IT} + 0.2 V,$	$V_{IL} = V_{IT} - 0.2 V$	6			μs
t _W	Pulse width	at MR	$V_{DD} \ge V_{IT} + 0.2 \text{ V},$ $V_{IH} = 0.7 \times V_{DD}$	$V_{IL} = 0.3 \times V_{DD}$	1			μs

switching characteristics at R $_L$ = 1 M $\Omega,\,C_L$ = 50 pF, T_A = 25 $^{\circ}C$

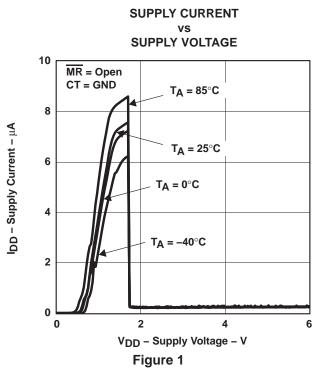
	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Delevitive		$\frac{V_{DD}}{MR} \ge V_{IT} + 0.2 \text{ V},$ $MR = 0.7 \times V_{DD},$ $CT = GND,$ See timing diagram	5	10	15	
^t d	Delay time		$\begin{split} &\frac{V_{DD}}{MR} \geq V_{IT} + 0.2 \text{ V,} \\ &MR = 0.7 \times V_{DD}, \\ &CT = V_{DD} \text{ ,} \\ &\text{See timing diagram} \end{split}$	100	200	300	ms
t _{PHL}	Propagation (delay) time, high-to-low-level output	V _{DD} to RESET delay	$V_{IL} = V_{IT} - 0.2 V,$ $V_{IH} = V_{IT} + 0.2 V$			10	μs
		(TPS3836, TPS3838)	V _{IL} = 1.6 V			50	
tPLH	Propagation (delay) time, low-to-high-level output	V _{DD} to RESET delay	$V_{IL} = V_{IT} - 0.2 V,$ $V_{IH} = V_{IT} + 0.2 V$			10	μs
		(TPS3837)	V _{IL} = 1.6 V			50	
tPHL	Propagation (delay) time, high-to-low-level output	MR to RESET delay (TPS3836, TPS3838)	$V_{DD} \ge V_{IT} + 0.2 \text{ V},$ $V_{IL} = 0.3 \times V_{DD},$			0.1	μs
^t PLH	Propagation (delay) time, low-to-high-level output	MR to RESET delay (TPS3837)	$V_{IL} = 0.7 \times V_{DD}$			0.1	μs

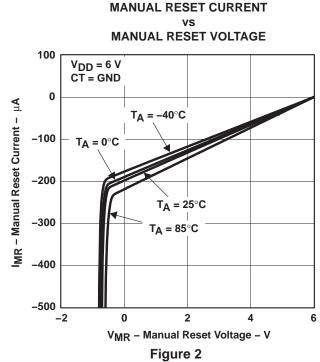
TYPICAL CHARACTERISTICS

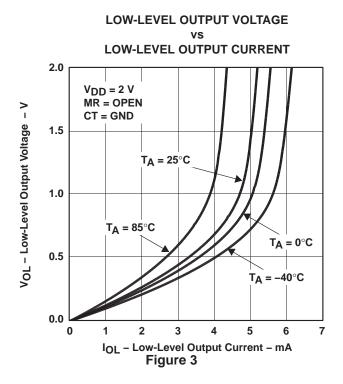
Table of Graphs

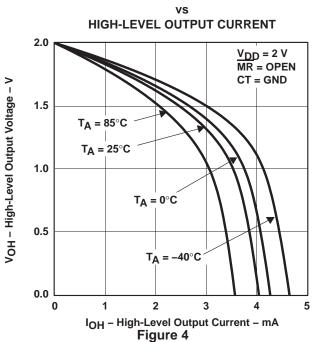
			FIGURE
I_{DD}	Supply current	vs Supply voltage	1
I _{MR}	Manual reset current	vs Manual reset voltage	2
VOL	Low-level output voltage	vs Low-level output current	3
Vон	High-level output voltage	vs High-level output current	4
	Normalized reset threshold voltage	vs Free-air temperature	5
	Minimum pulse duration at V _{DD}	vs V _{DD} Threshold overdrive	6

TYPICAL CHARACTERISTICS









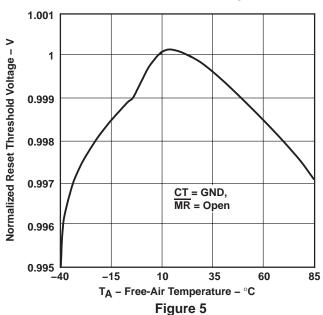
HIGH-LEVEL OUTPUT VOLTAGE

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TYPICAL CHARACTERISTICS

NORMALIZED RESET THRESHOLD VOLTAGE

FREE-AIR TEMPERATURE



MINIMUM PULSE DURATION AT V_{DD}

V_{DD} THRESHOLD OVERDRIVE

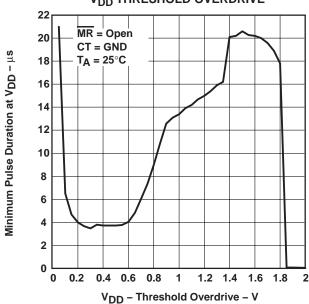


Figure 6







18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
2U3836E18QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3836H30QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3836J25QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3836K33QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3836L30QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3837E18QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3837J25QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3837K33QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3837L30QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3838E18QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3838J25QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3838K33QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
2U3838L30QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836E18QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3836H30QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3836J25QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3836K33QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3836L30QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3837E18QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3837J25QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3837K33QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3837L30QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3838E18QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838J25QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3838K33QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3838L30QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs. **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

18-Sep-2008

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3836E18-Q1, TPS3836H30-Q1, TPS3836J25-Q1, TPS3836K33-Q1, TPS3836L30-Q1, TPS3837E18-Q1, TPS3837J25-Q1, TPS3837K33-Q1, TPS3837L30-Q1, TPS3838E18-Q1, TPS3838J25-Q1, TPS3838K33-Q1, TPS3838L30-Q1

- Catalog: TPS3836E18, TPS3836H30, TPS3836J25, TPS3836K33, TPS3836L30, TPS3837E18, TPS3837J25, TPS3837K33, TPS3837L30, TPS3838E18, TPS3838J25, TPS3838K33, TPS3838L30
- Enhanced Product: TPS3836L30-EP, TPS3837K33-EP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



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